IN THE CLAIMS:

1. (currently amended) A data processing system comprising:

a memory for storing operands;

at least one general purpose register, wherein the memory does not include the at least one general purpose register; and

processor circuitry for executing one or more instructions, at least one of the one or more instructions for transferring data elements between the memory and the at least one general purpose register wherein one of the one or more instructions specifies: (a) a first offset between data elements within a first portion of successive data elements in the memory; (b) a first number of data elements to be transferred between the memory and the at least one GPR; and (c) a second offset between the first portion and a second portion of data elements in the memory,

wherein the data processing system further comprises a first general purpose register and a second general purpose register wherein the one of the one or more instructions transfers data elements between the memory and both the first general purpose register and the second general purpose registers in response to executing one of the one or more instructions, and wherein the one of the one or more instructions further specifies a total number of data elements to be transferred between the memory and both the first general purpose register and the second general purpose register.

2. (original) The data processing system of claim 1 wherein the one of the one or more instructions further specifies a data element size of the data elements in the memory.

3. (original) The data processing system of claim 1 wherein the one of the one or more instructions further specifies size of data elements in the memory separate and independent from specifying size of data elements in the at least one general purpose register.

4. (original) The data processing system of claim 3 wherein the processor circuitry determines a total number of data elements to be transferred based on size of data elements in the memory.

5 (original) The data processing system of claim 3 wherein the processor circuitry determines a total number of data elements to be transferred based on size of data elements in the at least one general purpose register.

6. – 8. (canceled).

9. (currently amended) The data processing system of claim [[8]] 1 wherein if the total number of data elements transferred does not completely fill the second general purpose register, the processor circuitry fills at least a portion of any remaining bit locations with a predetermined value.

10. (currently amended) The data processing system of claim [[7]] 1 wherein the one of the one or more instructions further separately specifies a number of data elements to be transferred between the memory and each of the first and second general purpose registers.

11. (canceled).

12. (original) The data processing system of claim 1 wherein the one of the one or more instructions further comprises a specifier wherein the second offset is used no more than once by the processor circuitry while transferring the first number of data elements.

13. (original) The data processing system of claim 12 wherein the processor circuitry communicates data elements in the memory by using a circular buffer when the one of the one or more instructions specifies that the second offset is to be used only once.

14. (original) The data processing system of claim 1 wherein the one of the one or more instructions further comprises a specifier wherein the second offset is used more than once by the

processor circuitry if the first number of data elements to be transferred is larger than twice the first portion of data elements to be transferred.

15. (canceled).

16. (currently amended) A method for using multiple addressing modes comprising:

providing a memory for storing operands;

providing at least one general purpose register, wherein the memory does not include the at least one general purpose register;

executing one or more instructions, at least one of the one or more instructions transferring data elements between the memory and the at least one general purpose register;

specifying with the at least one of the one or more instructions a first offset between data elements within a first portion of successive data elements in the memory;

specifying with the at least one of the one or more instructions a first number of data elements to be transferred between the memory and the at least one GPR; [[and]]

specifying with the at least one of the one or more instructions a second offset between the first portion and a second portion of data elements in the memory; and

providing a first general purpose register and a second general purpose register and transferring data elements between the memory and both the first general purpose register and the second general purpose registers in response to executing one of the one or more instructions, the method further comprising using the one of the one or more instructions to further specify a total number of data elements to be transferred between the memory and both the first general purpose register and the second general purpose register.

17. (original) The method of claim 16 further comprising:

using the at least one of the one or more instructions to further specify a data element size of the data elements in the memory.

18. (original) The method of claim 16 further comprising:

using the at least one of the one or more instructions to further specify size of data elements in the memory separate and independent from specifying size of data elements in the at least one general purpose register.

19. (original) The method of claim 16 further comprising using a processor to determine a total number of data elements to be transferred based on size of data elements in the memory.

20. (original) The method of claim 19 further comprising using the processor to determine a total number of data elements to be transferred based on size of data elements in the at least one general purpose register.

21. – 23. (canceled).

24. (currently amended) The method of claim [[22]] 16 further comprising filling at least a portion of any remaining unfilled bit locations in the second general purpose register with a predetermined value if a total number of data elements transferred does not completely fill the second general purpose register.

25. (currently amended) The method of claim [[21]] 16 further comprising using the one of the one or more instructions to further separately specify a number of data elements to be transferred between the memory and each of the first and second general purpose registers.

26. (canceled).

27. (original) The method of claim 16 further comprising providing a specifier in the one of the one or more instructions wherein in response to the specifier, the second offset is used only once by a processor transferring the first number of data elements.

28. (original) The method of claim 27 further comprising communicating data elements in the memory under control of the processor by using a circular buffer when the one of the one or more instructions specifies that the second offset is to be used only once.

29. (original) The method of claim 16 further comprising providing a specifier in the one of the one or more instructions wherein in response to the specifier, the second offset is used more than once by a processor if the first number of data elements to be transferred is larger than twice the number of data elements in the first portion of data elements in the memory.

30. (original) The data processing system of claim 16 further comprising providing a radix specifier in the one of the one or more instructions, the radix specifier implementing transfer of one or more data elements in a bit-reversed order between the memory and the at least one general purpose register.

31. – 42 (canceled).